PATENT APPLICATION
DOCKET NO.: 200208930-1

REMARKS

Claims 1-27 are currently pending, of which claims 1, 12, 17, 21, and 27 are in independent form.

Claims 1, 4, 11, 12, 17, 21, 24, and 27 have been amended. No new matter is introduced hereby.

Favorable consideration of the present application as currently constituted is respectfully requested.

Regarding the Specification

In the pending Office Action, the disclosure is objected to because of certain informalities. Responsive to the comments in connection therewith, Applicant has appropriately amended Paragraphs **[0001]**, **[0018]**, and **[0021]** of the original specification.

Regarding the Claim Rejections - 35 U.S.C. §102

In the pending Office Action, claims 1-27 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Pat. App. Publication No. 2002/0093356 in the name of Williams et al. (hereinafter the *Williams* reference). In connection with these

rejections, the Examiner has commented as follows with respect to the base claims 1, 12, 17, 21, and 27:

> As to claims 1, 12, 17, 21 and 27 Williams discloses:
> (1) A system for building a test case operable to test a circuit design, comprising:
> an instruction generation engine for generating a set of instructions (test vectors/test patterns/mask vectors), at least one of said instructions including a temporarily uncommitted (random/dynamic) value ([0006]-[0008]; [0032]; [0043]);
> a first summary generation engine (pseudo random number generator 230) portion for generating an interfaceable enumeration of said set of instructions (a reproducible sequence of pseudo random bits), wherein each said temporarily uncommitted values is denoted by an uncommitted reference ([0007]; [0038]); and
> a second summary generation engine (ATPG tool 12) portion for resolving respective values of said uncommitted references and generating an interfaceable listing of said uncommitted references and their said respective values ([0035]-[0037]),
> wherein said set of instructions and a summary including said interfaceable listing of said uncommitted references with resolved values are arranged to form said test case (vector) ([0039]; [0042]);
>
> (12), (17), (27) A method/computer-readable medium having stored program code/system for building a test case operable to test a circuit design, comprising ([0052]-[0055]):
> generating a set of instructions, at least one of said instructions including an expression having temporarily uncommitted value ([0006]-[0008]; [0032]; [0043]);
> generating an interfaceable enumeration of said set of instructions, wherein each of said temporarily uncommitted values is denoted by an uncommitted reference ([0007]; [0038]);
> resolving respective values of said uncommitted references ([0035]-[0037]);

generating an interfaceable listing of said uncommitted references and their said respective values ([0035]-[0037]); and

associating said set instructions with said interfaceable enumeration of said set of instructions and said interfaceable listing of resolved uncommitted references, thereby forming said test case ([0039]; [0042]);

(21) A computer system operable to simulate a platform for testing a circuit design, the computer system comprising:

a random number generator, operating responsive to a seed, for generating a random number sequence ([0019]);

an event probability generator, operating responsive to profile settings, for generating a probability profile (deterministic test vector data) ([0018]-[0019]; and

a test generator, operating responsive to said random number sequence and said probability profile, for generating a test case including a set of instructions and an interfaceable summary of said set of instructions ([0035]-[0037]; [0039]; [0042]),

wherein said set of instructions includes at least one expression having a temporarily uncommitted value that is resolved by said test generator and presented said interfaceable summary ([0039]; [0042]).

Applicant respectfully submits that the foregoing §102(b) claim rejections have been overcome or otherwise rendered moot by way of the present response. The embodiments as defined by the pending base claims 1, 12, 17, and 27 are directed to, *inter alia*, a system, method, and related computer-readable medium for building a test case operable to test a circuit design. Additionally, base claim 21 is directed to a computer system operable to simulate a platform for testing circuit design. As currently constituted, the

base claim 1 recites, *inter alia*, an instruction generation engine for generating a set of instructions comprising computational expressions, wherein at least one of the instructions includes a temporarily uncommitted value. Likewise, the currently amended base claim 12 recites, *inter alia*, generating a set of instructions comprising computational expressions, at least one of which includes a temporarily uncommitted value. Substantially identical features are also recited in the pending base claims of 17, 21, and 27.

The *Williams* reference discloses a method and circuit for testing an IC device using intelligent test vector formatting that reduces the storage required for test patterns. See Abstract. This is accomplished by providing a test vector mask that includes a deterministic portion as well as a random portion, which can be compressed. See, e.g., Paragraphs **[0035]-[0037]** and **[0043]-[0045]**. Test patterns are generated by a tester which selects deterministic bits as well as random bits under control of the test vector mask. See Paragraph **[0060]**. As exemplified in Paragraphs **[0006]-[0009]**, test vector patterns are comprised of binary data of certain length, with one or more "don't care" positions or none at all. Applicant respectfully submits that the test patterns, i.e., mere binary bit strings, of *Williams* do not anticipate or even remotely

suggest the claimed test case instructions comprising computational expressions, wherein at least one of the instructions includes a temporarily uncommitted value in an expression.

Accordingly, at least for the foregoing reasons, Applicant respectfully asserts that the pending base claims 1, 12, 17, 21, and 27 are allowable over *Williams*. Dependent claims 2-11 depend from the base claim 1 and introduce additional limitations therein. Therefore, dependent claims 2-11 are also believed to be in condition for allowance over the *Williams* reference. Likewise, dependent claims 13-16 depending from the base claim 12, dependent claims 18-20 depending from the base claim 17, and dependent claims 22-26 depending from the base claim 21 are also allowable over the applied art for the same reasons as set forth above.

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SUMMARY AND CONCLUSION

In view of the fact that none of the art of the record, whether considered alone or in combination discloses, anticipates or suggests the pending claims, and in further view of the above remarks and amendments, reconsideration of the Action and allowance of the present patent application are respectfully requested and are believed to be appropriate.

Respectfully submitted,

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